

**1024-BIT BIPOLAR RAM (1024X1)****82S10/82S110 (O.C.)****82S11/82S111 (T.S.)**

82S10/110-F,N • 82S11/111-F,N

**DESCRIPTION**

The 82S10/11, with a typical access time of 30ns, is ideal for cache buffer applications and for systems requiring very high speed main memory.

The 82S10/11 family requires single +5V power supply and features very low current pnp input structures. They include on-chip decoding and a chip enable input for ease of memory expansion, and feature either open collector or tri-state outputs for optimization of word expansion in bused organizations.

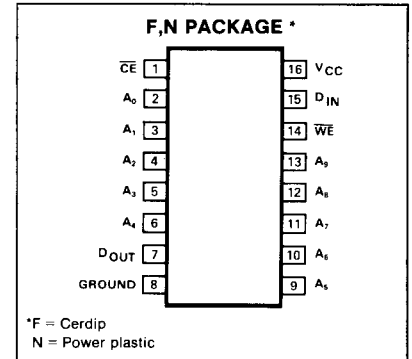
All devices are available in the commercial temperature range (0°C to +75°C) and are specified as N82S10/110/11/111. The 82S10 and 82S11 are also available in the military temperature range (-55°C to +125°C) and are specified as S82S10/11.

**FEATURES**

- **Address access time:**  
N82S10/11: 40ns max  
S82S10/11: 60ns max  
N82S110/111: 30ns max
- **Write cycle time:**  
N82S10/11: 40ns max  
S82S10/11: 60ns max  
N82S110/111: 30ns max
- **Power dissipation: 0.5W/bit typ**
- **Input loading:**  
N82S10/11: -250μA max  
S82S10/11: -250μA max  
N82S110/111: -250μA max
- **Output options:**  
82S10/110: Open collector  
82S11/111: Tri-state
- **On-chip address decoding**
- **Non-inverting output**
- **Blanked output during Write**
- **Fully TTL compatible**

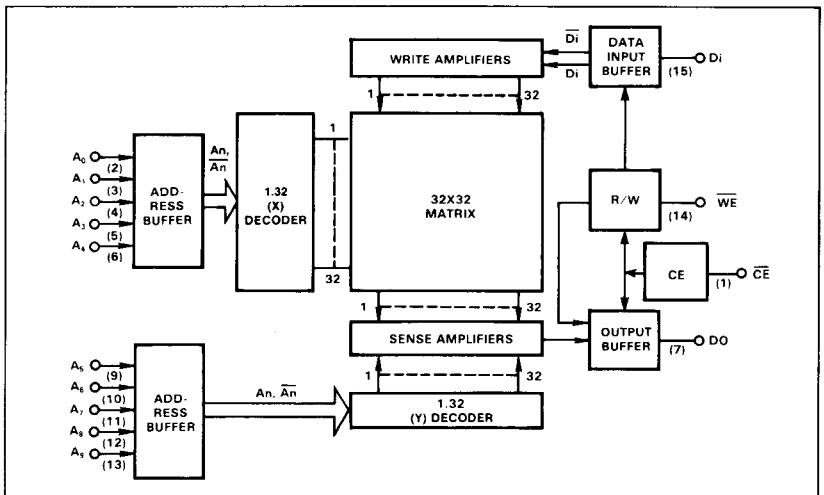
**APPLICATIONS**

- **High speed main frame**
- **Cache memory**
- **Buffer storage**
- **Writable control store**

**PIN CONFIGURATION****TRUTH TABLE**

MODE	$\overline{CE}$	$\overline{WE}$	D	D OUT	
				82S10/110	82S11/111
Read	0	1	X	Stored data	Stored data
Write "0"	0	0	0	1	High-Z
Write "1"	0	0	1	1	High-Z
Disabled	1	X	X	1	High-Z

X = Don't care.

**BLOCK DIAGRAM**

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**ABSOLUTE MAXIMUM RATINGS**

PARAMETER <sup>1</sup>	RATING	UNIT
V <sub>CC</sub> Supply voltage	+7	Vdc
V <sub>IN</sub> Input voltage	+5.5	Vdc
Output voltage		Vdc
V <sub>OH</sub> High (82S10/110)	+5.5	
V <sub>O</sub> Off-state (82S11/111)	+5.5	
T <sub>A</sub> Temperature range		°C
Operating	0 to +75	
N82S10/11/110/111	-55 to +125	
S82S10/11		
T <sub>STG</sub> Storage	-65 to +150	

**DC ELECTRICAL CHARACTERISTICS<sup>2</sup>** N82S10/110/11/111: 0°C ≤ T<sub>A</sub> ≤ +75°C, 4.75V ≤ V<sub>CC</sub> ≤ 5.25V  
 S82S10/11: -55°C ≤ T<sub>A</sub> ≤ +125°C, 4.5V ≤ V<sub>CC</sub> ≤ 5.5V

PARAMETER	TEST CONDITIONS	N82S10/11/110/111			S82S10/11			UNIT
		Min	Typ <sup>3</sup>	Max	Min	Typ <sup>3</sup>	Max	
V <sub>IL</sub> Input voltage Low <sup>1</sup>	V <sub>CC</sub> = Min			.85				V
V <sub>IH</sub> Input voltage High <sup>1</sup>	V <sub>CC</sub> = Max	2.1			2.1			V
V <sub>IC</sub> Input voltage Clamp <sup>1,4</sup>	V <sub>CC</sub> = Min, I <sub>IN</sub> = -12mA		-1.0	-1.5		-1.0	-1.5	V
V <sub>OL</sub> Output voltage Low <sup>1,5</sup>	V <sub>CC</sub> = Min, I <sub>OL</sub> = 16mA		0.35	0.45		0.35	0.50	V
V <sub>OH</sub> Output voltage High (82S11/111) <sup>1,6</sup>	I <sub>OH</sub> = -2mA	2.4			2.4			V
I <sub>IL</sub> Input current Low	V <sub>IN</sub> = 0.45V		-10	-250		-10	-250	μA
I <sub>IH</sub> Input current High	V <sub>IN</sub> = 5.5V		1	25		1	40	μA
I <sub>OLK</sub> Output current Leakage (82S10/110) <sup>7</sup>	V <sub>CC</sub> = Max, V <sub>OUT</sub> = 5.5V		1	40		1	60	μA
I <sub>O(OFF)</sub> Output current Hi-Z state (82S11/111)	V <sub>OUT</sub> = 5.5V		1	60		1	100	μA
I <sub>OS</sub> Output current Short circuit (82S11/111) <sup>8</sup>	V <sub>OUT</sub> = 0.45V <sup>7</sup> , V <sub>OUT</sub> = 0V	-20	-1	-60	-20	-1	-100	mA
I <sub>CC</sub> V <sub>CC</sub> supply current <sup>9</sup>	V <sub>CC</sub> = Max, 0 < T <sub>A</sub> < 25°C, T <sub>A</sub> ≥ 25°C, T <sub>A</sub> ≤ 0°C		120, 95	155, 130, 170		120, 95	155, 130, 170	mA
C <sub>IN</sub> Capacitance Input	V <sub>CC</sub> = 5.0V, V <sub>IN</sub> = 2.0V		7			4		pF
C <sub>OUT</sub> Capacitance Output	V <sub>OUT</sub> = 2.0V							pF

**BIPOLAR MEMORY**

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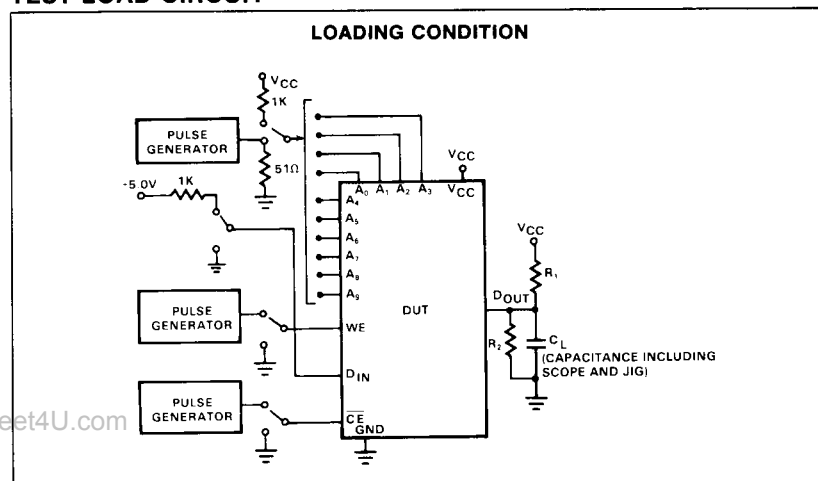
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**AC ELECTRICAL CHARACTERISTICS<sup>2</sup>**  $R_1 = 270\Omega$ ,  $R_2 = 600\Omega$ ,  $C_L = 30\text{pF}$ N82S10/110/11/111:  $0^\circ\text{C} \leq T_A \leq +75^\circ\text{C}$ ,  $4.75\text{V} \leq V_{CC} \leq 5.25\text{V}$ S82S10/11:  $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$ ,  $4.5\text{V} \leq V_{CC} \leq 5.5\text{V}$ 

PARAMETER	TO	FROM	N82S10/11			N82S110/111			S82S10/11			UNIT
			Min	Typ <sup>3</sup>	Max	Min	Typ	Max	Min	Typ <sup>3</sup>	Max	
Access time $T_{AA}$ Address $T_{CE}$ Chip enable				30	40			30		30	60	ns
Disable time $T_{CD}$ $T_{WD}$	Output Output	Chip enable Write enable		15	30			25		15	45	ns
$T_{WR}$ Write recovery time				20	30			25		20	45	ns
Setup and hold time $T_{WSA}$ Setup time $T_{WHA}$ Hold time	Write enable	Address	5 5	0		5			15 10	0		ns
$T_{WSD}$ Setup time $T_{WHD}$ Hold time	Write enable	Data in	30 5	25		25			55	35		ns
$T_{WSC}$ Setup time $T_{WHC}$ Hold time	Write enable	$\overline{CE}$	5	0		5			5	0		ns
Pulse width $T_{WP}$ Write enable <sup>10</sup>			30	25		20			50	25		ns

**NOTES**

- All voltage values are with respect to network ground terminal.
- The operating ambient temperature ranges are guaranteed with transverse air flow exceeding 400 linear feet per minute and a 2-minute warm-up.  
Typical thermal resistance values of the package at maximum temperature are:  
 $\theta_{JA}$  junction to ambient at 400fpm air flow -  $50^\circ\text{C}/\text{watt}$   
 $\theta_{JA}$  junction to ambient - still air -  $90^\circ\text{C}/\text{watt}$   
 $\theta_{JA}$  junction to case -  $20^\circ\text{C}/\text{watt}$
- All typical values are at  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ .
- Test each input one at a time.
- Measured with a logic low stored. Output sink current is supplied through a resistor to  $V_{CC}$ .
- Measured with  $V_{IL}$  applied to  $\overline{CE}$  and a logic high stored.
- Measured with  $V_{IH}$  applied to  $\overline{CE}$ .
- Duration of the short circuit should not exceed 1 second.
- $I_{CC}$  is measured with the write enable and memory enable inputs grounded, all other inputs at 4.5V, and the output open.
- Minimum required to guarantee a Write into the slowest bit.

**TEST LOAD CIRCUIT****VOLTAGE WAVEFORM**